CLAIMS

What is claimed is:

1. In a computer network having a plurality of network nodes, a method for buffering packets comprising:

receiving a packet incoming from said network;

randomly selecting a particular memory module from a plurality of memory modules coupled in parallel;

storing said packet in said particular memory module.

2. The method of Claim 1 further comprising the step of queuing said packet in a queue corresponding to the particular memory module.

3. The method of Claim 1 further comprising the step of reading data from said plurality of memory modules in a random order by which said data was written to said plurality of memory modules.

4. The method of Claim 1 wherein said memory modules comprise DRAM memory.

5. The method of Claim 1, wherein said DRAM memory comprise 5Gps bandwidth.

6. The method of Claim 1, wherein said plurality of memory modules comprise SRAM memory.

7. The method of Claim 1, wherein delays corresponding to writing data into said plurality of memory modules can be described by a binomial distribution.

8. An apparatus, comprising:

a plurality of memories coupled in parallel;

a scheduler coupled to said plurality of memories, wherein the scheduler randomly selects which of said memories data is to be written.

9. The apparatus of Claim 8 further comprising a plurality of queues coupled to the plurality of memories, wherein said scheduler directs a data packet to one of said plurality of queues randomly.

10. The apparatus of Claim 8, wherein delay associated with writing data to the plurality of memories can be described by a binomial distribution.

11. The apparatus of Claim 8, wherein said plurality of memories comprise DRAM memory modules.

12. The apparatus of Claim element of Claim 8, wherein said plurality of memories comprise SRAM memory modules.

13. A system, comprising:

a plurality of memories;

a memory controller coupled to said plurality of memories, wherein data is written to random locations of said plurality of memories.

14. The system of Claim 13, wherein the plurality of memories are coupled in parallel and total memory bandwidth equals a sum of memory bandwidths of said plurality of memories.

15. The system of Claim 13, wherein packets from a network are queued and stored in randomly selected memory modules of said plurality of memories.

16. The system of Claim 15, wherein said plurality of memory modules comprise DRAM memories.

17. The system of Claim 13, wherein worst-case memory access latency is minimized.

18. The system of Claim 13, wherein worst-case memory access latency is controlled by a binomial distribution.

19. The system of Claim 13, wherein a probability that a memory is selected to read/write a packet into is randomly uniformly distributed.

20. The system of Claim 13, wherein a probability that at least x of n requests will be written to a module comprise a binomial distribution function.